IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A data processor, comprising~~, at least,~~:

a CPU ~~for controlling~~ configured to control an entire system[[,]];

a DSP ~~for performing~~ configured to perform preset processing, to have at least two bus cycles in a unit of one data access, and to use a selectable number of the bus cycles in the unit of one data access; [[,]] and

an external memory configured to be accessed by the DSP and to be ~~capable of being~~ accessed through the DSP by the CPU[[;]], wherein

~~the DSP being configured to have at lease two bus cycles as a unit of one data access,~~

~~the number of the bus cycles used in the unit of one data access being selectable, and~~

a data word length ~~to be~~ accessed by the DSP at [[to]] the external memory ~~being~~ is variable[[;]], and

the DSP includes ~~including:~~

a determination ~~means for determining~~ unit configured to determine whether the DSP is accessing [[to]] the external memory ~~or not~~;

a control ~~means for determining~~ unit configured to determine whether the CPU is allowed to access the external memory, based on ~~the presence and absence of~~ a signal from [[a]] the determination unit ~~means~~; and

~~means for performing~~ a switching unit configured to perform a switching operation of an address and a data in connection with the external memory according to a command from the control ~~means~~ unit, and ~~inputting or outputting~~ to input and to output the address and the data based on the switching operation[[;]].

wherein ~~in a case where~~ when the data word length is selected so ~~as to perform accessing by~~ that the DSP accesses the external memory using a maximum number of the bus cycles, when the determination ~~means~~ unit determines that the DSP is accessing the external memory, access from the CPU to the external memory is placed in a wait state by the control unit ~~means~~, and

~~in a case where~~ when the data word length is not selected so ~~as to perform accessing by a~~ that the DSP accesses the external memory using the maximum number of the bus cycles, the control ~~means allows~~ unit is configured to allow the CPU to access the external memory by utilizing a free bus cycle.

2. (Currently Amended) A data processor, comprising~~, at least,~~:

a CPU ~~for controlling~~ configured to control an entire system[[,]];

a sound source ~~for supplying~~ configured to supply a musical tone signal[[,]];

a DSP ~~for performing~~ configured to perform preset processing to apply a desired effect to the musical tone signal supplied from the sound source, to have at least two bus cycles in a unit of one data access with respect to signal processing of the musical tone signal, and to use a selectable number of bus cycles in the unit of one data access [[,]]; and

an external memory configured to be accessed by the DSP and to be ~~capable of being~~ accessed through the DSP by the CPU[[;]], wherein

~~the DSP being configured to have at lease two bus cycles as a unit of one data access with respect to signal processing of the musical tone signal,~~

~~the number of the bus cycles used in the unit of one data access selectable, and~~

a data word length ~~to be~~ accessed by the DSP at [[to]] the external memory ~~being~~ is variable[[;]], and

the DSP includes ~~including:~~

a determination ~~means for determining~~ unit configured to determine whether the DSP is accessing [[to]] the external memory ~~or not~~;

a control ~~means for determining~~ unit configured to determine whether the CPU is allowed to access the external memory, based on ~~the presence and absence of~~ a signal from [[a]] the determination unit ~~means~~; and

~~means for performing~~ a switching unit configured to perform a switching operation of an address and a data in connection with the external memory according to a command from the control means, and ~~inputting or outputting~~ to input and to output the address and the data based on the switching operation, [[;]]

wherein ~~in a case where~~ when the data word length is selected so ~~as to perform accessing by~~ that the DSP accesses the external memory using a maximum number of the bus cycles, when the determination ~~means~~ unit determines that the DSP is accessing the external memory, access from the CPU to the external memory is placed in a wait state by the control unit ~~means~~, and

~~in a case where~~ when the data word length is not selected so ~~as to perform accessing by a~~ that the DSP accesses the external memory using the maximum number of the bus cycles, the control ~~means allows~~ unit is configured to allow the CPU to access the external memory by utilizing a free bus cycle.

3. (Currently Amended) A data processor having a fixed number of memory access timings per sampling cycle, the data processor [[and]] comprising:

a plurality of DSPs ~~for accessing~~ configured to access a single external memory in a single package;

~~the data processor further comprising:~~

an access determination unit configured to determine, when each of the DSPs issues a read command or a write command at a same time, which one of the DSPs is allowed to access the memory;

a read/write control ~~means~~ unit configured to control, ~~which~~ when each of the DSPs issues [[a]] the read command or [[a]] the write command at the same ~~timing~~ time, ~~controls the~~ a command of ~~which~~ the allowed DSP ~~is allowed~~;

~~an access determination means, which when each of the DSPs issues a read command or a write command in the timing, determines which DSP is allowed to perform memory access;~~

a first selector ~~for outputting~~ configured to output an address from the allowed DSP in response to a determination signal from the access determination ~~means~~ unit; and

a second selector ~~for outputting a~~ configured to output data from the allowed DSP in response to the determination signal[[; and]], wherein

each of the DSPs ~~including~~ includes a control ~~means for data acquisition, which acquires a~~ unit configured to acquire data from the external memory in response to the determination signal from the access determination ~~means~~ unit.

4. (Currently Amended) The data processor according to Claim 3, wherein the read/write control ~~means~~ unit does not access the external memory when each of the ~~respective~~ DSPs ~~issue plural commands~~ simultaneously issues a command.

5. (Currently Amended) A data processor having a fixed number of memory access timings per sampling cycle, the data processor [[and]] comprising:

a plurality of DSPs ~~for accessing~~ configured to access a single external memory in a single package, the external memory storing musical tone waveform data;

~~the data processor further comprising:~~

an access determination unit configured to determine, when each of the DSPs issues a read command or a write command at a same time, which one of the DSPs is allowed to access the memory;

a read/write control ~~means~~ unit configured to control, ~~which~~ when each of the DSPs issues [[a]] the read command or [[a]] the write command at the same ~~timing~~ time, ~~controls~~ the command of ~~which~~ the allowed DSP ~~is allowed~~;

~~an access determination means, which when each of the DSPs issues a read command or a write command in the timing, determines which DSP is allowed to perform memory access;~~

a first selector ~~for outputting~~ configured to output an address from the allowed DSP in response to a determination signal from the access determination ~~means~~ unit; and

a second selector ~~for outputting a~~ configured to output data from the allowed DSP in response to the determination signal[[; and]], wherein

each of the DSPs ~~including~~ includes a control ~~means for data acquisition, which acquires a~~ unit configured to acquire data from the external memory in response to the determination signal from the access determination ~~means~~ unit.

6. (Currently Amended) The data processor according to Claim 5, wherein the read/write control ~~means dose~~ unit does not access the external memory when each of the ~~respective~~ DSPs ~~issue plural commands~~ simultaneously issues a command.